REMARKS/ARGUMENT

Claims 4-5, 8-15, 17-20 and 24-40 stand rejected under 35 U.S.C. 112, second paragraph. By this amendment, Claims 4, 8, 10, 17, 18, 28, 37 and 38 have been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejections. 5 and 16-20 have been amended to include the limitations of Claim 1 and any intervening claims. As such, Claims 4, 5 and 16-20 are now allowable.

1) Claim 16 stands rejection under 35 U.S.C. 103(a) as being unpatentable over Simon et al (GB 2230627) in view of Arvidsson et al (US 6,414,627). Applicants respectfully traverse this rejection as follows:

Independent Claim 1, as amended, requires and positively recites a discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors.

Simon discloses a recursive processor that is used as a first order section IIR filter. To obtain a "cascaded" second or third order section IIR filter, more processors coupled together in cascaded form are required. Examiner admits that Simon does not teach or suggest that the filters comprise solely of switches and capacitors (Office Action, page 3, lines 20-21). Examiner relies upon Arvidsson et al as suggesting a IIR filter comprising solely switches (K1-K5, S1-S5) and capacitors (C1-C5) for obtaining a variable value switches capacitor with drastically reduced number of capacitors. Examiner goes on to argue that it would have been obvious to a person having skill in the art at the time the invention was made to employ the switches and capacitors as suggested by Arvidsson et al

in Simon et al for the purpose of obtaining a variable switched capacitor with drastically reduced number of capacitors.

Applicants respectfully point out that there is no teaching in Simon that would lead one having ordinary skill in the art that its second order filter comprising a cascaded single pole IIR filter ((50, 50', 50")) use, or would likely use, switch capacitor circuits in its second order filter. Arvidsson et al., on the other hand, specifically states that its invention is related to switched capacitor circuits, where resistor and inductors are replaced by switches and capacitors. There is no teaching in either reference that teaches or suggests a combination of the two technologies.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention**

is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). It is clear from the above analysis that the Examiner has not met his burden of **showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.** As such, a prima facie case of the obviousness of Claim 16 over a combination of Simon and Ardvisson has not been shown.

Claims 2, 3, 6-15 stand allowable as depending directly, or indirectly, from allowable Claim 16 and by including further limitations not taught or suggested by the references of record.

Claim 2 further defines the discrete time analog filter according to claim 16, by further comprising **means for direct sampling**, wherein **the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers.** In addition to being allowable for depending from allowable claim 16, Claim 2 is further allowable over any combination of Simon and Ardvisson since the references alone, or in combination, fail to teach or suggest, and "**means for direct sampling**" and "wherein **the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers**". Accordingly, Claim 2 is allowable.

Claim 3 further defines the discrete time analog filter according to claim 2, wherein the means for direct sampling comprises a multi-tap direct sampling mixer. Claim 3 stands allowable for the same reasons set forth above in support of the allowance of Claim 16.

Applicants appreciate the Examiner indication that Claims 4-15, 17-20 and 24-40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in the Office action and to include all of the limitations of the base claim and any intervening claims. By this amendment the above identified claims have been amended to overcome the 35 U.S.C. 112, second paragraph, rejections. Accordingly, Claims 17-20 and 24-40 stand allowable. Claims 4-15, as amended, are allowable in their present form since they depend directly, or indirectly, from allowable Claim 16.

2) Claim 16 stands rejection under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 5,732,002) in view of Arvidsson et al (US 6,414,627). Applicants respectfully traverse this rejection as follows:

Independent Claim 1, as amended, requires and positively recites a discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors.

Lee discloses multi-rate IIR decimation and interpolation filters. Examiner admits that Lee does not teach or suggest that the filters comprise solely of switches and capacitors (Office Action, page 4, lines 10-11). Examiner relies upon Arvidsson et al as suggesting a IIR filter comprising solely switches (K1-K5, S1-S5) and capacitors (C1-C5) for obtaining a variable value switches capacitor with drastically reduced number of capacitors. Examiner goes on to argue that it would have been obvious to a person having skill in the art at the time the invention was made to employ the switches and capacitors as suggested by Arvidsson et al in Lee et al for the purpose of obtaining a variable switched capacitor with drastically reduced number of capacitors.

Applicants respectfully point out that there is no teaching in Lee that would lead one having ordinary skill in the art that its cascaded single pole IIR filters (14, 16, 18, 20) use, or would likely use, switch capacitor circuits. Arvidsson et al., on the other hand, specifically states that its invention is related to switched capacitor circuits, where resistor and inductors are replaced by switches and capacitors. There is no teaching in either reference that teaches or suggests a combination of the two technologies.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

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Claims 2, 3, 6-15 stand allowable as depending directly, or indirectly, from allowable Claim 16 and by including further limitations not taught or suggested by the references of record.

Claim 2 further defines the discrete time analog filter according to claim 16, by further comprising **means for direct sampling**, wherein **the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers**. In addition to being allowable for depending from allowable claim 16, Claim 2 is further allowable over any combination of Simon and Ardvisson since the references alone, or in combination, fail to teach or suggest, and **"means for direct sampling"** and "wherein **the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers**". Accordingly, Claim 2 is allowable.

Claim 3 further defines the discrete time analog filter according to claim 2, wherein the means for direct sampling comprises a multi-tap direct sampling mixer. Claim 3 stands allowable for the same reasons set forth above in support of the allowance of Claim 16.

Applicants appreciate the Examiner indication that Claims 4-15, 17-20 and 24-40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in the Office action and to include all of the limitations of the base

claim and any intervening claims. By this amendment the above identified claims have been amended to overcome the 35 U.S.C. 112, second paragraph, rejections. Accordingly, Claims 17-20 and 24-40 stand allowable. Claims 4-15, as amended, are allowable in their present form since they depend directly, or indirectly, from allowable Claim 16.

Accordingly, Claims 1-20 and 24-24 stand allowable. Applicants respectfully request withdrawal of the rejections and allowance of the application as the earliest possible date.

Respectfully submitted,

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